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An Efficient Analytical Inductor Core Loss Calculation Method for Two-level and Three-level PWM Converters based on a User-friendly Loss Map

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Abstract—This paper proposes an efficient analytical approach to calculate the inductor core loss for Pulse Width Modulation (PWM) converters with the aid of a pre-built, user-friendly core loss map. Loss map is the most practical approach to accurately estimate the core loss of an inductor exposed to PWM operation. To predict the inductor core loss, the inputs of the loss map needs to be retrieved from the steady-state inductor voltage/current waveforms. For estimation purpose, an analytical approach is proposed in this paper, which enables mathematical and simplified computation of the operating space and core loss of the inductor in a PWM converter. The proposed approach is developed for both 2-level and 3-level converters and then validated by experiments. The results indicate that a 3-level converter operates the same inductor with less core loss compared to a 2-level converter, when the maximum current ripple is kept equivalent by halving the switching frequency in the 3-level converter.

Keywords—core loss, loss map, Pulse Width Modulation, three level converters, two level converters

I. INTRODUCTION

Inductors play an important role in power electronics, which have unneglectable contribution to the volume and power loss of Pulse Width Modulation (PWM) converters [1]. Estimation of inductor loss is important in achieving an accurate system-level modelling, which is beneficial in the design and optimization of a PWM power converter in terms of efficiency and power density. The power loss of an inductor consists of two parts: copper loss and core loss. While the copper loss can be accurately estimated by analytical models (e.g. [2]), the core loss is more difficult to predict in PWM converters [3]–[7]. The particular difficulties in the case of inductor core loss in PWM converters are caused by PWM operations, which involves dc-bias (pre-magnetization) [5], varying pulse widths and square-wave excitation. In this case, core loss modelling can only rely on empirically tested data, while the existing datasheets of magnetic cores are only based on sinusoidal excitation without considering the dc-bias effect.

To tackle the challenges in core loss estimation for PWM converters, a practical approach is to build up a “loss map” based on empirical B-H loop measurements [3], [6]. Loss map is a database that covers possible operating points of the inductor core described by all identified factors. The loss map approach

is formed by two stages: (1) establish the loss map (2) utilize the loss map to calculate core loss. For estimation purpose, the inputs of the loss map, i.e. the steady-state PWM waveforms, need to be retrieved. One approach is to draw the waveforms from a simulation model [8]. But time-domain simulations are time-consuming and difficult to be integrated into mathematical models and iterative optimization tools such as [9].

Hence, it is motivated to generate the inputs analytically for core loss estimation. There are previous studies that presented analytical approaches of estimating the core loss, such as [10]–[13]. However, [10], [13] are based on Steinmetz Equation (SE) and Improved Generalized Steinmetz Equation (IGSE), which have not considered the effect of pre-magnetization. In addition, these studies mainly focused on the line inductors in 2-level Power Factor Correction (PFC) converters. In recent years, 3-level converters, such as the Neutral Point Clamped (NPC) [14] and T-type converter (TNPC) converters [15], are drawing attentions both in academia and industry for low and medium voltage applications. Hence, this paper also investigates the 3-level converters in terms of the inductor core loss.

The contribution of this paper is the approach to analytically calculate the inductor core loss in PWM converters, with the aid of a pre-measured, user-friendly loss map. This approach can achieve efficient estimation of the core loss of inductors in both 2-level and 3-level converters. Additionally, the proposed approach can be easily integrated into an analytical, system-level modelling/optimization of a power converter. This paper will be presented in the following sequence: (1) user-friendly loss map (2) analytical core loss calculation approach (3) experimental evaluation.

II. LOSS MAP APPROACH

A. B-H loop measurement

To characterize the core loss of an inductor, B-H loop measurement is widely used in previous studies [3], [5], [7]. As the most important feature of this approach, only the core loss is measured out from the total inductor losses. To perform B-H loop measurement, an additional flux sensing winding is fitted on the inductor. The principle of this approach is to find the magnetic field H and flux density B on the inductor core by measuring the excitation current I and the open-circuit voltage on the sensing coil U_{L2} , as expressed in (1) and (2).

$$B(t) = \frac{1}{N_2 A_e} \int_0^T U_{L2}(t) dt \quad (1)$$

$$H(t) = \frac{N_1 \cdot I(t)}{l_e} \quad (2)$$

Where N_1 is the number of turns of the main winding of the inductor; N_2 is the number of turns of the flux-sensing winding; A_e is the effective cross-section area of the core; l_e is the effective length of magnetic path of the core. The core loss can then be found from the B-H domain by (3).

$$Q = A_e l_e \int H dB = \frac{N_1}{N_2} \int_0^T I(t) \cdot U_{L2}(t) dt \quad (3)$$

A top-level illustration of the setup to perform B-H loop measurement is shown in Fig. 1.

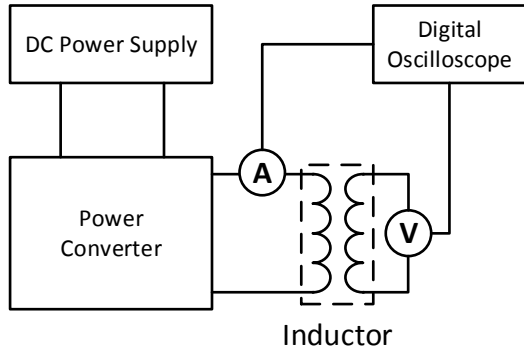


Fig. 1. B-H loop measurement setup

To drive the excitation current into the inductor-under-test, a power converter is required. According to [7], a half-bridge structure with the DC-link formed by two adjustable power supplies in series is preferred for the power converter stage. This configuration allows the excitation current to flow in both directions and enables the compensation of asymmetric inductor voltage caused by the voltage drops on power devices. Note the accuracy of B-H loop measurement is sensitive to the phase discrepancy between the current and voltage probes [3], [16]. In this study, the phase discrepancy of the probes is calibrated through a de-skew tool Keysight U1880A.

B. User-friendly Loss Map

Considering the rectangular excitation voltage and DC-bias effect, loss map is the most practical approach to accurately estimate the core loss of an inductor for PWM operations ([3], [6]). Loss map is a database of pre-measured core losses covering operating points defined by three variables as shown in (4): flux density change rate $|dB/dt|$, swing of flux density ΔB and dc-biased magnetic field strength H_0 .

$$P_v = f\left(\left|\frac{dB}{dt}\right|, \Delta B, H_0\right) \quad (4)$$

For an individual inductor, the loss map in magnetic/time domain can be converted into electrical/time domain following equations (5)-(7), assuming $U_{L1}/U_{L2} = N1/N2$.

$$H_0 = \frac{1}{T_{ab}} \cdot \frac{N_1}{l_e} \int_a^b i(t) dt = I_0 \cdot \frac{N_1}{l_e} \quad (5)$$

$$\frac{dB}{dt} = \frac{1}{T_{ab}} \frac{1}{N_2 A_e} \int_a^b U_{L2}(t) dt = U_L \cdot \frac{1}{N_1 A_e} \quad (6)$$

$$\Delta B = \frac{1}{N_2 A_e} \int_a^b U_{L2}(t) dt = U_L \cdot T_{ab} \cdot \frac{1}{N_1 A_e} \quad (7)$$

Where $N1/N2$ is the turn ratio, U_{L1}/U_{L2} are the primary/secondary voltages; T_{ab} is the period of one B-H loop. Consequently, the three inputs of the loss map can be converted into the form expressed by (8)

$$Q = f(U_L T, U_L, I_0) \quad (8)$$

Since the core loss profile varies from inductor to inductor ([7], [17]), this study focuses on one specific inductor that has been built and tested. A Triple Pulse Test (TPT) procedure [7] is applied to build up the loss map in this study. The tested inductor is a customized, high-current inductor with gapped CoFe EE cores. Fig. 2 shows the converted user-friendly loss map of this inductor.

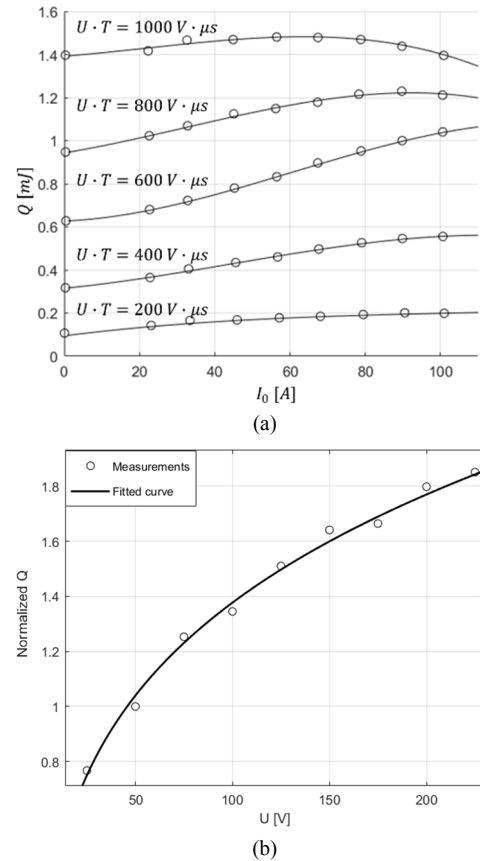


Fig. 2. User-friendly loss map (a) Q vs. $U_L \cdot T$ and I_0 ($U_L = 50$ V) (b) Q vs. U_L normalized to 50 V [7]

A pre-measured loss map enables the estimation of the high-frequency core loss of the tested inductor. If the inductor voltage and current from PWM operations are given, a method can be

applied to calculate the core loss out from the built loss map [7]. This loss map calculation firstly decomposes the PWM excitation into half-loop segments, which are separated by the zero-crossings of inductor voltage u_L . Fig. 3 illustrates an example of one segment. For each segment, the associated core loss can be found from the loss map by feeding the three inputs (as in (8)) extracted from this segment. Assuming the given PWM waveform is formed by n pieces of segments, the total core loss over the given period is calculated by adding up the core losses of all n segments.

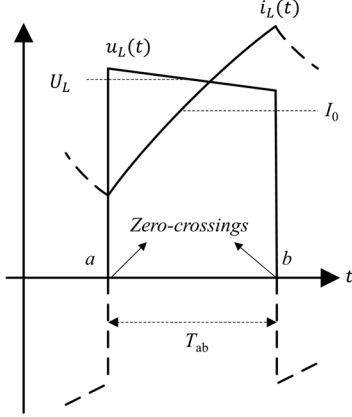


Fig. 3. A segment for core loss calculation ($U_L > 0$)

III. ANALYTICAL CORE LOSS ESTIMATION

Considering the pre-measured loss map as the datasheet of the inductor, this datasheet can be utilized to estimate the inductor core loss in a PWM power converter. The high-frequency inductor losses can be significant [3] and therefore needs to be considered in the system-level modelling of a power converter. As introduced, to estimate the core loss, the steady-state inductor voltage/current waveforms are required. These waveforms can be obtained from simulations for estimation purpose. But the time-domain simulations are time-consuming, especially in the case of performing iterative optimization, such as [9]. Alternatively, the core loss estimation can be conducted analytically and mathematically. This section intends to develop an efficient analytical method to calculate the core loss utilizing the pre-measured user-friendly loss map.

A. Analytical model with a 2-level converter

To start with, a single-phase, two-level, grid-connected Static Synchronous Compensator (STATCOM) system is considered as an example, which is shown in Fig. 4.

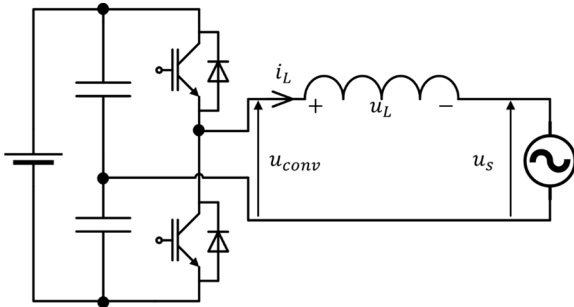


Fig. 4. Grid-tied single-phase two-level STATCOM

From the grid-frequency point of view, the phasor relationships of the currents/voltages in this system can be derived as plotted in Fig. 5. It assumes the ideal operation of the STATCOM, which only drives reactive current into the grid with the power losses in the converter neglected.

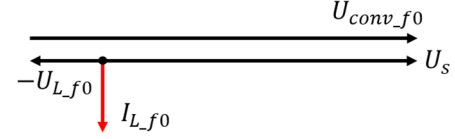


Fig. 5. Phasor diagram of an ideal STATCOM system exporting reactive power

From the inductor point of view, the operation of the system can then be represented by Fig. 6 [18]. The converter on one side is generating varying-duty-cycle square waves on switching window basis. On the other side, the grid is a stable source of sinusoidal voltage u_s with a frequency of f_0 .

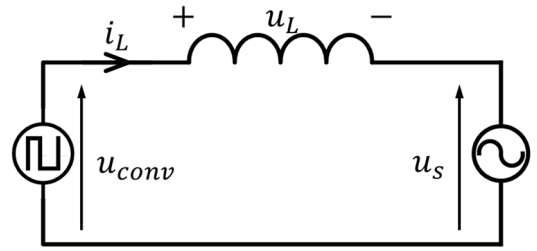


Fig. 6. Equivalent circuit for core loss calculation

In this equivalent circuit, the inductor voltage u_L is found from the converter output voltage u_{conv} and the grid voltage u_s as

$$u_L(t) = u_{conv}(t) - u_s(t) \quad (9)$$

Another representative example is a converter-fed passive load with a LC low-pass filter as shown in Fig. 7.

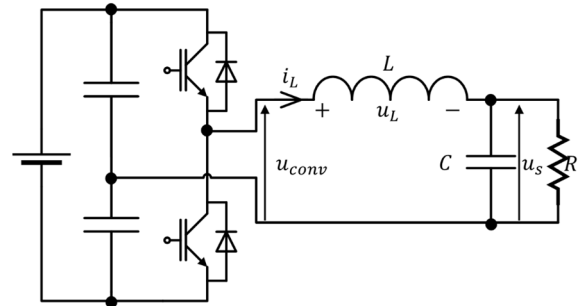


Fig. 7. Two-level inverter with a passive load and low-pass LC filter

The phasor diagram of this configuration can be derived as in Fig. 8.

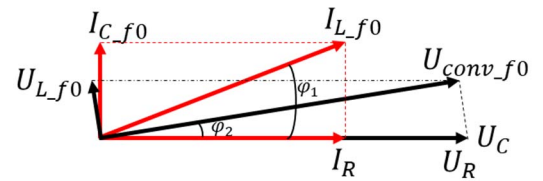


Fig. 8. Phasor diagram of converter with RLC load at fundamental frequency

For simplification, it can also be assumed that the filtered load voltage U_R is sinusoidal. In this case, the operation of the inductor can also be represented by the equivalent circuit shown in Fig. 6.

In Fig. 6, Assuming the converter switching frequency $f_{sw} \gg f_0$, the grid/load voltage u_s can be treated as constant in each switching window. Subsequently, the converter voltage and grid voltage in one switching window is considered as illustrated in Fig. 9 (a). In the +DC cycle, the converter outputs $+U_{DC}/2$. In the -DC cycle, the converter outputs $-U_{DC}/2$. Following (9), the inductor voltage u_{L+}/u_{L-} in each switching window can be found by (10) and (11) for +DC/-DC cycles respectively, as illustrated in Fig. 9(b).

$$U_{L+} = \frac{U_{DC}}{2} - U_s \quad (10)$$

$$U_{L-} = -\frac{U_{DC}}{2} - U_s \quad (11)$$

In order to utilize the user-friendly loss map (8), the three inputs must be found for each segment, which are $U_L T$, U_L and I_0 . As mentioned, the segments are separated by the zero crossings of the inductor voltage u_L . As shown in Fig. 9(b), the instants zero-crossings of u_L can be treated the same as the converter voltage. Therefore, in one switching window, the +DC cycle corresponds to the positive segment; the -DC cycle corresponds to the negative segment.

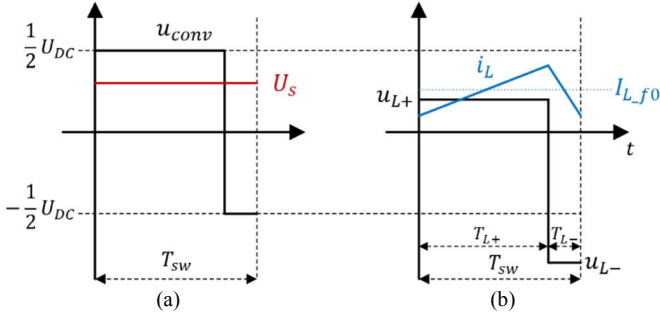


Fig. 9. Example of a 2-level converter in one switching window ($U_{ref} > 0$) (a) converter output voltage, grid/load voltage (b) inductor voltage/current

The time duration and duty cycles of u_{conv} can be found from the reference voltage of the converter, which is U_{conv_f0} . Assuming conventional Sinusoidal Pulse Width Modulation (SPWM) is applied, the duty cycles of the +DC/-DC cycles in one switching window can be calculated by (12), (13). And the time durations are found from the duty cycles by (14).

$$D_{L+} = [\frac{U_{conv_f0}}{(U_{DC}/2)} + 1]/2 \quad (12)$$

$$D_{L-} = 1 - D_{L+} \quad (13)$$

$$T_{L+/L-} = D_{L+/L-} \cdot \frac{1}{f_{sw}} \quad (14)$$

The DC-bias current I_0 for the segments can also be found from the fundamental component of the inductor current I_{L_f0} as

shown in Fig. 9(b). The I_{L_f0} can be derived from the phasor diagram shown in Fig. 5.

Following the above process, the three inputs of segments for the user-friendly loss map can be generated on switching window basis. In order to find the averaged core loss, the above process needs to be repeated for each switching window over one fundamental cycle. This process can be achieved by performing iterations in a numerical computing software, such as MATLAB. The whole process is visualized in Fig. 10.

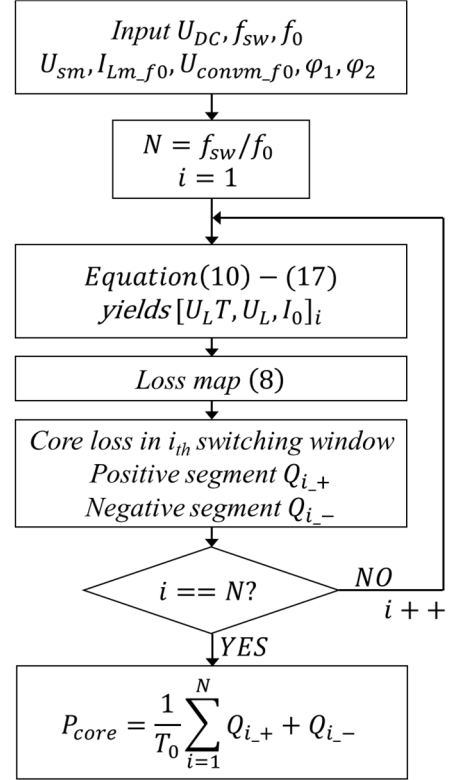


Fig. 10. Core loss computation process

As an example, assuming $f_0 = 100$ Hz and $f_{sw} = 20$ kHz, one fundamental cycle can be sliced up to $N = 200$ switching windows. Each switching window contains one positive segment and one negative segment (unless T_{+DC} or T_{-DC} equals to zero when the peak reference voltage reaches the modulation boundaries). For the i_{th} ($i = 1 \dots N$) switching window, three fundamental-frequency components are expressed by (15)-(17), with the phase angle referenced to the load/grid voltage.

$$U_s = U_{sm} \cdot \sin(\frac{i}{N} \cdot 2\pi) \quad (15)$$

$$I_{L_f0} = I_{Lm_f0} \cdot \sin(\frac{i}{N} \cdot 2\pi + \phi_1) \quad (16)$$

$$U_{conv_f0} = U_{convm_f0} \cdot \sin(\frac{i}{N} \cdot 2\pi + \phi_2) \quad (17)$$

Where U_{sm} , I_{Lm_f0} , U_{convm_f0} are the amplitudes of the fundamental-frequency load/grid voltage, inductor current and converter output voltage; ϕ_1 and ϕ_2 are the phase angles. All

these constants can be found from the operating model of the converter and the load, i.e. the phasor diagrams Fig. 5 and Fig. 8. By inputting (10)-(17) into the loss map (8), the core loss of the i_{th} switching window can be calculated, which contains the core loss for the positive segment Q_{i+} and the negative segment Q_{i-} in the form of energy.

Finally, the core losses of all switching windows are summed up to yield the total core loss of one fundamental cycle. Subsequently, the averaged core loss in power P_L can be obtained.

To summarize, for the analytical core loss estimation, the operation of the inductor is found by the equivalent circuit shown in Fig. 6 at switching window level. To extract the inputs for the calculation, the amplitudes and phase relationships of the fundamental-frequency component of U_{conv_f0} , I_{L_f0} and U_s are found from the operating model of the converter and the load. These inputs associated with the converter/load operation are similar to the required parameters in the analytical estimation of the power losses of power devices, such as [19]–[21]. This feature enables the proposed core loss estimation to be directly integrated into an analytical, system-level modelling and optimization of a power converter, such as [9], [22].

Note the proposed approach only relies on the prediction of the converter output voltage rather than the instantaneous current ripple prediction at switching period level. Current ripple prediction (e.g. [18], [23]) assumes that the inductance L is constant for simplification. The presented approach will bypass the uncertainty of instantaneous inductance L at high frequencies. Additionally, the converter output voltage is easier to model in the discussed Voltage Source Converters (VSCs).

B. Analytical model with a 3-level converter

The above proposed analytical approach can be extended to a 3-level converter. A 3-level converter outputs three voltage levels: positive DC rail voltage U_{+DC} , neutral point voltage U_{NP} and negative DC rail voltage U_{-DC} . With SPWM applied, in each switching window the ideal converter output voltage is formed by U_{+DC}/U_{NP} when $U_{ref} > 0$, or U_{-DC}/U_{NP} when $U_{ref} < 0$. Therefore, the inductor voltage is still a two-level square-wave within each switching window as shown in Fig. 11, shifted up/down due to the grid/load side voltage.

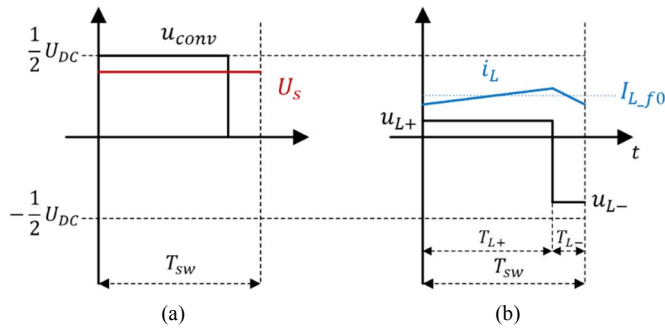


Fig. 11. Example of a 3-level converter in one switching window ($U_{ref} > 0$) (a) converter output voltage, grid/load voltage (b) inductor voltage/current

Fig. 9 shows a comparison of the inductor voltage/current waveforms in a 2-level and a 3-level converter with the same switching frequency f_{sw} .

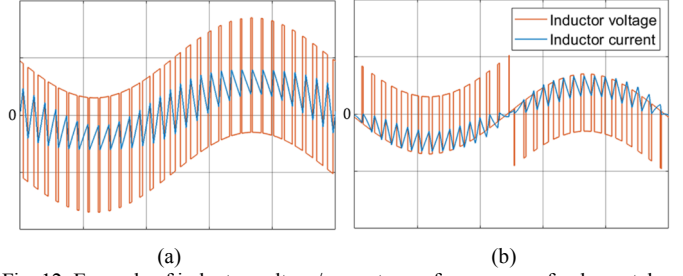


Fig. 12. Example of inductor voltage/current waveforms over a fundamental cycle (a) 2-level converter (b) 3-level converter

The duty cycles in a 3-level converter can be derived from the reference voltage as following. When $U_{conv_f0} \geq 0$, the duty cycles and inductor voltages are calculated from (18)-(21)

$$D_{+DC} = U_{conv_f0} / (U_{DC}/2) \quad (18)$$

$$D_{NP} = 1 - D_{+DC} \quad (19)$$

$$U_{L+} = \frac{U_{DC}}{2} - U_s \quad (20)$$

$$U_{L-} = 0 - U_s \quad (21)$$

When $U_{conv_f0} \leq 0$, the duty cycles and inductor voltages are calculated from

$$D_{-DC} = -U_{conv_f0} / (U_{DC}/2) \quad (22)$$

$$D_{NP} = 1 - D_{-DC} \quad (23)$$

$$U_{L+} = 0 - U_s \quad (24)$$

$$U_{L-} = -\frac{U_{DC}}{2} - U_s \quad (25)$$

Hence, by replacing equations (10)-(13) with (18)-(25) in the calculation flow in Fig. 10, the core loss of the inductor in a 3-level converter can also be calculated.

IV. EXPERIMENTAL EVALUATION

A test rig is built for both the loss mapping process and the inverter operation to validate the proposed calculation method. The purpose is to investigate whether the operating space and core loss of the inductor can be correctly predicted by the presented analytical model.

The RLC load is configured as Fig. 7 with the specifications listed in Table 1. The power module SKiM301TMLI12E4B is based on a 3-level T-type topology, which allows the operation either as a 2-level converter or a 3-level converter. This enables a straightforward comparison between these two converter

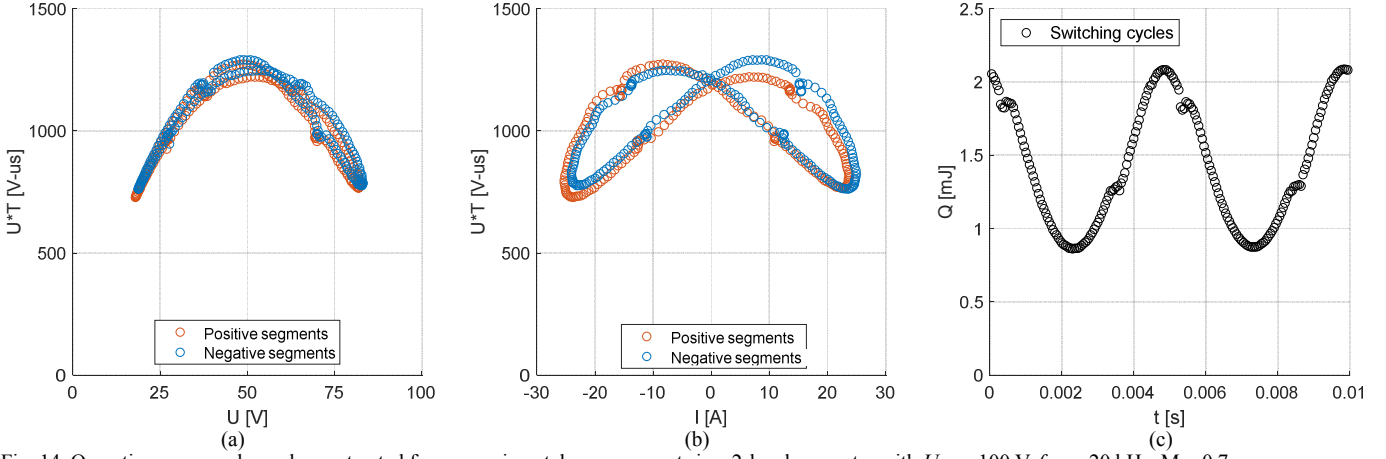


Fig. 14. Operating space and core loss extracted from experimental measurements in a 2-level converter with $U_{DC} = 100$ V, $f_{sw} = 20$ kHz, $M = 0.7$
(a) $U_L \cdot T$ and U_L (b) $U_L \cdot T$ and I_0 (c) Core loss

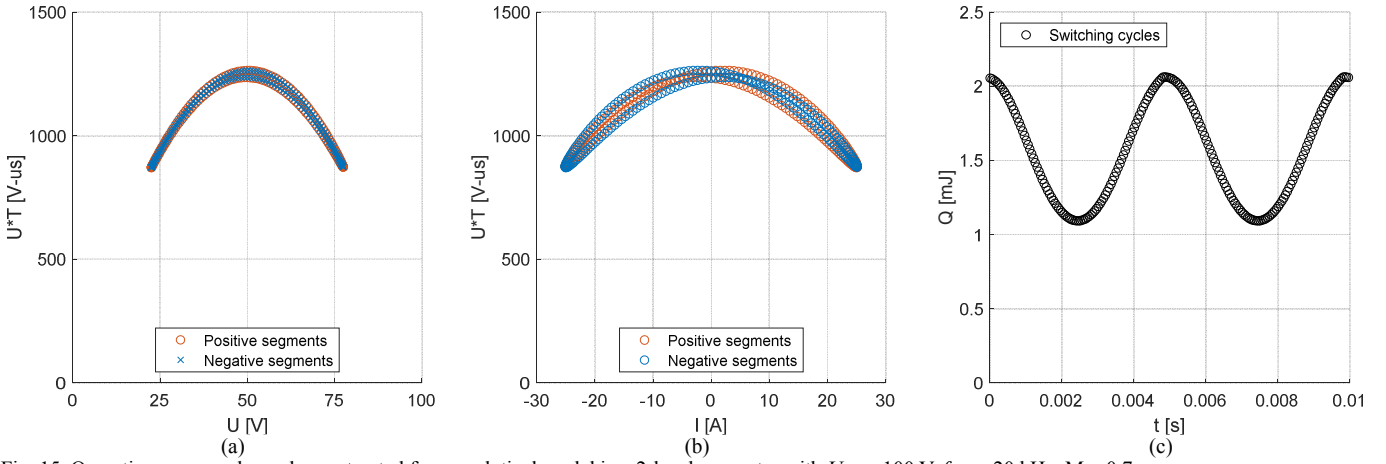


Fig. 15. Operating space and core loss extracted from analytical model in a 2-level converter with $U_{DC} = 100$ V, $f_{sw} = 20$ kHz, $M = 0.7$
(a) $U_L \cdot T$ and U_L (b) $U_L \cdot T$ and I_0 (c) Core loss

topologies regarding the inductor core loss. A picture of the setup is shown Fig. 13.

Table 1 Specifications of the test rig

Fundamental frequency f_0	100 Hz	R	1.1 Ω
Switching frequency f_{sw}	10 kHz/20 kHz	L	36 μ H
Dead time	2 μ s	C	135 μ F

Table 2 Components and instruments in the test rig

Power supply	EA-PS 8360-15 T	Power module	Semikron SKiM301TMLI12E4B
Digital Oscilloscope	MSO-X 3054A (500 MHz, 4 GSa/s)	Gate Driver	Semikron SKYPER 42 J
Voltage probe	Keysight N2862B (150 MHz)	Current probe	Keysight N2783B (100 MHz)

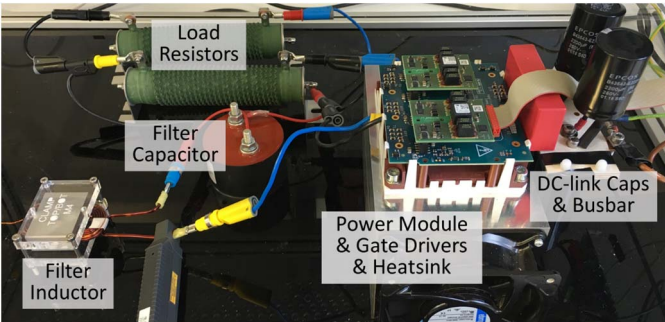


Fig. 13. Picture of the test setup

The inductor voltage and current are measured by high bandwidth probes and captured in the digital oscilloscope shown in Table 2.

The power converter is programmed to operate as two setups: (A) a 2-level converter with $f_{sw} = 20$ kHz; (B) a 3-level converter with $f_{sw} = 10$ kHz. Commonly, the inductance of the filter inductor in the discussed configuration is designed based on the maximum peak-to-peak current ripple $\Delta I_{MAXpk-pk}$ [9]. According to [23], a three-level converter offers approximately half the $\Delta I_{MAXpk-pk}$ compared to a two-level converter when the other parameters are the same. Therefore, if the same inductor is used, a three-level converter with $0.5f_{sw}$ can be considered equivalent to a two-level converter with f_{sw} from the $\Delta I_{MAXpk-pk}$ point of view. Hence, setup (A) and (B) provides a comparison between these two topologies on the same inductor with the $\Delta I_{MAXpk-pk}$ of both setups maintained equal.

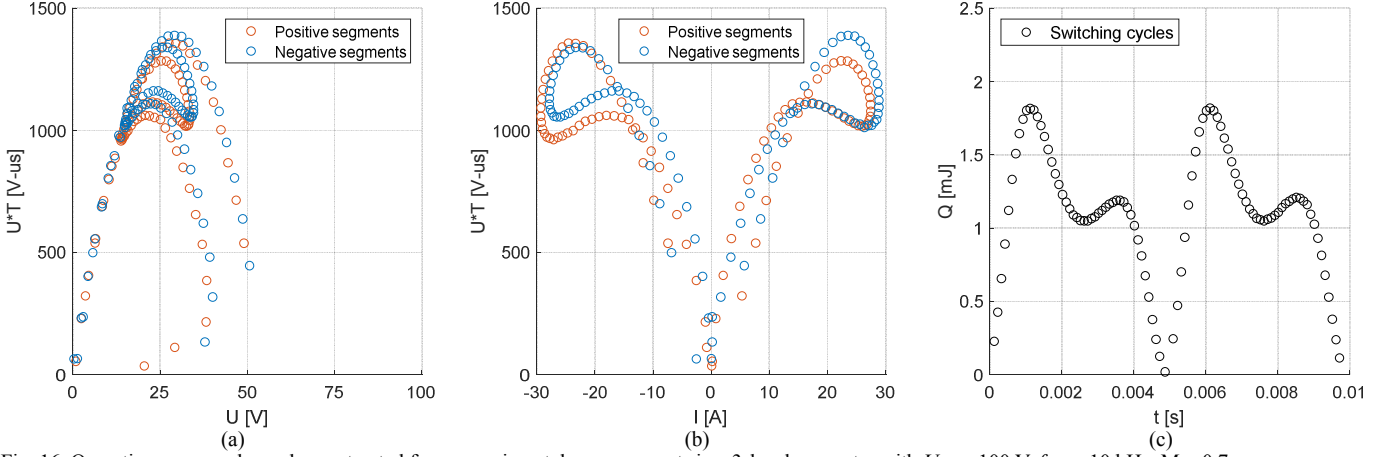


Fig. 16. Operating space and core loss extracted from experimental measurements in a 3-level converter with $U_{DC} = 100$ V, $f_{sw} = 10$ kHz, $M = 0.7$
(a) $U_L \cdot T$ and U_L (b) $U_L \cdot T$ and I_0 (c) Core loss

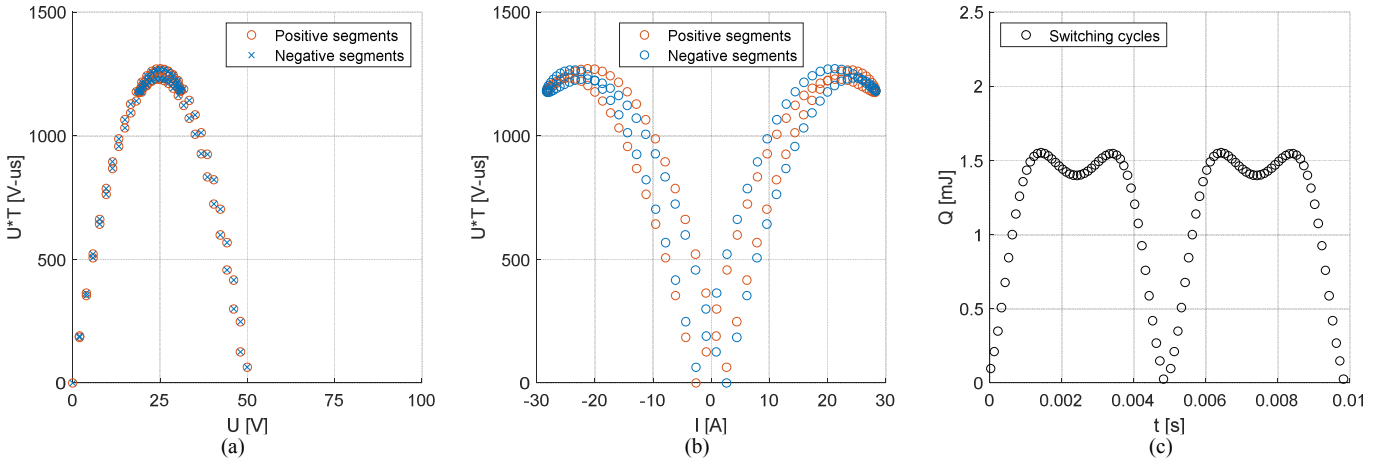


Fig. 17. Operating space and core loss extracted from analytical model in a 3-level converter with $U_{DC} = 100$ V, $f_{sw} = 10$ kHz, $M = 0.7$
(a) $U_L \cdot T$ and U_L (b) $U_L \cdot T$ and I_0 (c) Core loss

The experimental waveforms are measured and analyzed through the loss map calculation process. The results are visualized in Fig. 14 and Fig. 16 for the 2-level and 3-level setups respectively. Fig. 14(a)(b) shows the operating space of the inductor core with respect to the three inputs of the loss map. Fig. 14(c) shows the core loss calculated from the experimental waveform through the loss map approach.

In order to verify the proposed model, the parameters of the test rig are fed into the calculation flow presented in Section III to estimate the operating space and loss of the core. The analytically calculated results are plotted in Fig. 15 and Fig. 17. A comparison of the averaged core loss in two setups is shown in Table 3.

Table 3 Comparison of averaged core loss

	Experimental	Analytical
Setup (A)		
2-level, $f_{sw} = 20$ kHz	28.5 W	31.0 W
Setup (B)		
3-level, $f_{sw} = 10$ kHz	10.6 W	11.4 W

Table 3 indicate that the core loss derived experimentally agrees well with the theoretical results. The analytical model yields slightly higher core loss than the experimental results. It is also clear that the core loss in the 3-level case is only approximately one third of the number in the 2-level case.

Comparing Fig. 14 and Fig. 15, it can be seen that both the operating space and the instantaneous core loss are well predicted by the analytical model in the 2-level setup. The result shows that the core loss has two peaks over one fundamental cycle.

Fig. 16 and Fig. 17 indicate that the theoretical estimation also agrees with the experimental results in the 3-level setup, although there are visible discrepancies. These discrepancies are mainly caused by the non-ideal operation of the power converter and the load.

Comparing the operating space in the 2-level and 3-level cases, the following findings can be observed. Given the same inductor, the halved switching frequency in the 3-level setup leads to a similar peak $U_L T$ product as the 2-level setup, which is around 1250 V-us. This means the maximum current ripple $\Delta I_{MAXpk-pk}$ are kept the same in the two cases as expected. From the amplitude of U_L point of view, it is clear that in the 3-level converter U_L of segments concentrated at around 25 V and reaches maximum at only 50 V. In the 2-level case, U_L spreads between 25 V to 80 V. Additionally, in the 3-level setup, there are a number of switching cycles where the inductor operates with low $U_L T$ product, e.g. < 500 V-us. In the meantime, the $U_L T$ product in the 2-level setup are all above 750 V-us. Furthermore,

the number of switching cycles is twice in the 2-level converter to achieve the same peak current ripple. All these factors lead to the much smaller inductor core loss in the 3-level converter as indicated in Table 3.

The discrepancy between the theoretical model and the experimental results are mainly caused by the following non-ideal factors of the setup:

- Dead-time effect.
- Trapezoidal converter output voltage instead of ideal square wave.
- Additional resistances in the converter-load loop, which is neglected in the presented model for simplicity.
- Fluctuation of the dc-link voltage and neutral point voltage. The dc-link voltages are assumed constant in the theoretical model while they fluctuate in the test rig.

V. CONCLUSION

This paper proposed an efficient analytical approach of estimating the inductor core loss in PWM converters, with the aid of a pre-built, user-friendly loss map. The approach is elaborated based on two representative PWM converter-load configurations, a STATCOM system and a passive load system with a LC low-pass filter. The calculations are developed for both 2-level converters and 3-level converters. The experimental results indicated that the proposed approach is able to correctly predict the operating plane and core loss of the inductor.

As indicated by the results, a 3-level converter operates the same inductor with much less core loss compared to a 2-level converter, when the maximum current ripple is kept equivalent by halving the switching frequency in the 3-level converter.

The presented approach can be easily implemented in mathematical tools, such as MATLAB. It enables a efficient process of estimating the core loss of the inductors, which is beneficial for the system-level modelling and optimization of modern power electronics converters.

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